

REMARKS

At the time of the Office Action dated May 20, 2004, claims 1-12 were pending. Applicants acknowledge, with appreciation, the Examiner's indication that claim 9 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

In this Amendment, claims 1-3 and 10-12 have been canceled without prejudice. Claims 4-9 are active in this application.

Claims 1-4, 6-7 and 10-12 have been rejected under 35 U.S.C. §102(e) as being anticipated by Shin.

In the statement of the rejection, the Examiner asserted that Shin discloses a data processor identically corresponding to what is claimed. This rejection is respectfully traversed. It is noted that the rejection of claims 1-3 and 10-12 has been rendered moot by the cancellation of those claims.

It is established that the factual determination of lack of novelty under 35 U.S.C. §102 requires the identical disclosure in a single reference of each element of the claimed invention, such that the identically claimed invention is placed into the possession of one having ordinary skill in the art. *Helifix Ltd. v. Blok-Lok, Ltd.*, 208 F. 3d 1339, 54 USPQ2d 1299 (Fed. Cir. 2000); *Electro Medical Systems S.A. v. Cooper Life Sciences, Inc.*, 34 F.3d 1048, 32 USPQ2d 1017 (Fed. Cir. 1994). Although this disclosure requirement presupposes the knowledge of one skilled in the art of the claimed invention, that presumed knowledge does not grant a license to read into the prior art references teachings that are not there. *Motorola, Inc. v. Interdigital Tech. Corp.*, 121 F.3d 1461, 43 USPQ2d 1481 (Fed. Cir. 1997).

In response, Applicants submit that Shin does not disclose a data processor including all the limitations recited in independent claim 4 within the meaning of 35 U.S.C. §102. Specifically, Applicants stress that the Examiner's interpretation of Shin is not supported by the description of the reference.

Shin is directed to a controller for controlling read and write operations to reduce power consumption. In more detail, when greater than a half of the bits of input data to be written to DRAMs have a logic "low" value ("0"), a memory controller 31 sets a flag bit D_flag to a logic "low" level ("0"), and writes the inverted input data into the DRAMs. On the other hand, when fewer than a half of the bits of the input data have a logic "low" value ("0"), the memory controller 31 sets the flag bit D_flag to a logic "high" level ("1"), and writes the input data as is into the DRAMs. See column 4, lines 30-46.

In paragraph 2 of the Office Action, the Examiner asserted that Shin's input buffer part 420 in Fig. 4 corresponds to the claimed first retain circuit, and Shin's input conversion part 410 corresponds to the claimed subtracter. According to the Examiner, Shin's input buffer part 420 stores previous data output by a processing unit (not shown). The input conversion part 410 takes a difference between the previous data stored in the input buffer part 420 and current data output by the processing unit. However, there is no reason to interpret that Shin discloses what the Examiner asserted.

In fact, Shin discloses that the input conversion part 410 detects states of bits of a write data DQ_IN, converts a flag bit D_flag into a logic "low" or "high," and converts the write data DQ_IN (see column 4, line 66 to column 5, line 9). Shin does not teach that the input conversion part 410 receives data other than "write data DQ_IN," i.e., does not receive any data from the input buffer part 420. Moreover, the reference does not disclose that the input conversion part 410 takes "a

difference between the previous data stored in said retain circuit and current data output by said processing unit,” as recited in claim 4. Fig. 5 of Shin apparently shows that the input conversion part 410 merely includes a data comparison unit 411 and a data conversion unit 413, but does not include any unit for subtraction.

Further, the reference discloses that the input buffer part 420 buffers the data signal DIN and the flag bit D_flag0 outputted from the input conversion part 410, and outputs them to a plurality of Rambus DRAMs 32-32n (column 5, lines 9-12). There is no description in Shin that the input buffer part 420 provides “previous data” to the input conversion part 410.

Accordingly, the Examiner’s interpretation of Shin is not supported by its description. Therefore, Applicants submit that the Examiner did not discharge the initial burden of establishing a *prima facie* basis to deny patentability to the claimed invention under 35 U.S.C. §102 for lack of novelty. Moreover, it is apparent from the above discussion that Shin does not disclose a data processor including all the limitations recited in independent claim 4, and therefore, does not have identical disclosure of each element of the claimed invention in the meaning of 35 U.S.C. §102.

It is also noted that a dependent claim is not anticipated if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claim. Therefore, claims 6 and 7 are patentable because they respectively include all the limitations of independent claim 4. The Examiner’s additional comments with respect to claims 6 and 7 do not cure the argued fundamental deficiencies of the Examiner’s reason of the rejection of claim 4 as well as Shin.

Applicants, therefore, respectfully solicit withdrawal of the rejection of the claims and favorable consideration thereof.

Claims 5 and 8 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Shin, in view of Takahashi et al. and further in view of Igarashi et al.

In the statement of the rejection, the Examiner asserted that the proposed combination of Shin, Takahashi et al. and Igarashi et al. teaches and suggests a data processor including all the limitations recited in claims 5 and 8. Applicants respectfully traverse this rejection.

Applicants submit that the Examiner has not established a *prima facie* basis to deny patentability to the claimed invention under 35 U.S.C. §103 for lack of the requisite factual basis. To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974).

Based on the above legal tenet, Applicants submit that the proposed combination does not teach or suggest a data processor including all the limitations recited in claims 5 and 8. Specifically, Applicants emphasize that Shin does not disclose what is claimed in claim 1, on which claims 5 and 8 depend, for the reasons set forth above. Moreover, since Takahashi et al. and Igarashi et al. are directed merely to image compression methods, those two references do not cure fundamental deficiencies of Shin.

Therefore, the proposed combination of Shin, Takahashi et al. and Igarashi et al. does not teach or suggest each and every limitation of claims 5 and 8. In the instant case, the pending rejection has not established *prima facie* obviousness of the claimed invention as recited in claims 5 and 8, because the proposed combination fails to satisfy the requirement under §103. *See In re Royka*, 490 F.2d 981. Applicants, therefore, respectfully solicit withdrawal of the rejection of claims 5 and 8, and favorable consideration thereof.

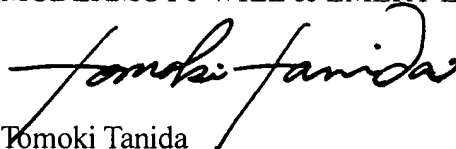
Conclusion.

Accordingly, it is urged that the application is in condition for allowance, an indication of which is respectfully solicited. If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, Examiner is requested to call Applicants' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

MCDERMOTT WILL & EMERY LLP

A handwritten signature in black ink, appearing to read "Tomoki Tanida", written over a horizontal line.

Tomoki Tanida

Recognition under 37 C.F.R. 10.9(b)

600 13th Street, N.W.
Washington, DC 20005-3096
202.756.8000 SAB:TT:lnm
Facsimile: 202.756.8087
Date: August 18, 2004

**BEFORE THE OFFICE OF ENROLLMENT AND DISCIPLINE
UNITED STATES PATENT AND TRADEMARK OFFICE**

LIMITED RECOGNITION UNDER 37 CFR § 10.9(b)

Mr. Tomoki Tanida is hereby given limited recognition under 37 CFR §10.9(b) as an employee of McDermott, Will & Emery to prepare and prosecute patent applications in which the patent applicant is the client of McDermott, Will & Emery and the attorney or agent of record in the applications is a registered practitioner who is a member of McDermott, Will & Emery. This limited recognition shall expire on the date appearing below, or when whichever of the following events first occurs prior to the date appearing below: (i) Mr. Tomoki Tanida ceases to lawfully reside in the United States, (ii) Mr. Tomoki Tanida's employment with McDermott, Will & Emery ceases or is terminated, or (iii) Mr. Tomoki Tanida ceases to remain or reside in the United States on an H-1B visa.

This document constitutes proof of such recognition. The original of this document is on file in the Office of Enrollment and Discipline of the U.S. Patent and Trademark Office.

Expires: June 1, 2006



Harry I. Moatz

Director of Enrollment and Discipline

RECEIVED

AUG 24 2004

Technology Center 2100